AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to FIG. 1. This sheet, which includes FIG. 1, replaces the original sheet including FIG. 1. In FIG. 1, the label "Prior Art" has been added.

Attachment: Replacement Sheet

REMARKS

These remarks are in response to the Final Office Action dated November 7, 2006 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1, 11, and 21 have been amended to clarify various aspects of the present invention. Support for these amendments can be found at paragraphs 25-33, 40, FIGs. 2-6, and throughout the Applicants' specification. Claims 1-2, 4-12, 14-22, and 24-30 remain pending. No new matter has been introduced.

In the Office Action, the drawings have been objected to for not including a legend such as "Prior Art" for FIG. 1. Applicants have attached a replacement drawing sheet including FIG. 1 with a legend that states "Prior Art". Withdrawal of the objection to the drawings is respectfully requested.

Claims 1-2, 4-12, 14-22, and 24-30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,779,169 to Singh et al. (Singh). The Applicants respectfully disagree with this rejection and contend that Singh fails to teach or suggest the Applicants' invention as recited in the claims.

Singh teaches a method of positioning components of a circuit design on a target device in which the components are grouped into different logic regions. (*See* column 3, lines 6-7, *stating* "a user (designer) may define logic regions that group certain components of a system together"). One shape is found for each logic region. (*See* column 4, lines 18-20, *stating* "a shape is found that will fit the components assigned to the logic region"). Each logic region, having an associated shape, is positioned on the target device. The shape of a logic region can be resized to facilitate the movement of the logic region during floorplanning. The resizing is predicated upon the location to which the logic region will be moved. (*See* column 6, lines 61-63, *stating* "[t]o make this move, the location of logic region 901 is extended outwards until it is the same size of logic region 902 as shown by dotted region 910").

The Applicants' invention, as recited in independent claims 1, 11, and 21, defines modules of a circuit design, determines a set of static shapes for each module prior to annealing, and anneals the circuit design using the shapes. For each module during a first iteration of annealing, a shape is selected from the set of static shapes associated with the module. The selected shape is applied to the module. For at least

one module during at least one further iteration of annealing, a different shape is selected from the set of shapes associated with the at least one module. The different shape is applied to the at least one module.

Accordingly, Singh determines a single shape for each logic region and adjusts the size of that shape as needed during placement. By comparison, the Applicants' invention generates a set of static shapes for each module prior to annealing. The shapes are static in that the size of each shape is not changed once determined, as is the case with Singh. For a given module, a different shape from the set of shapes associated with that module is selected and applied to the module during a further iteration of annealing. Nowhere does Singh teach or suggest that a plurality of shapes is determined for each module or that different shapes from the set of shapes associated with a module are selected and applied to that module during different iterations of annealing.

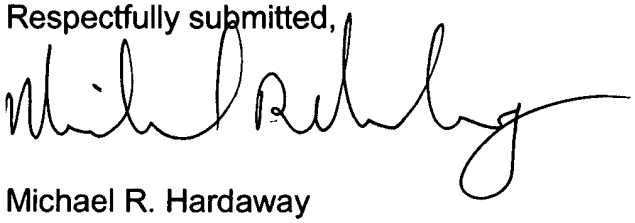
As Singh fails to teach or suggest the features recited in Applicants' claims, withdrawal of the 35 U.S.C. § 102(e) rejection with respect to claims 1-2, 4-12, 14-22, and 24-30 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,



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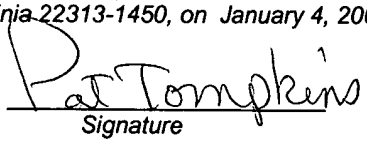
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 4, 2007.

Pat Tompkins
Name



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